a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein the impurity region is not in contact with the drain region, and

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region formed under the channel forming region and in the source region.

2-14. (Canceled)

15. (Original) A device according to claim 1, wherein the semiconductor device is an integrated circuit (IC).

16-17. (Canceled)

18. (Original) A device according to claim 1, wherein the semiconductor device is a microprocessor.

19-20. (Canceled)

21. (Original) A device according to claim 18, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

22-23. (Canceled)

24. (Original) A device according to claim 1, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

25-26. (Canceled)

27. (Canceled) A device according to claim 1, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

28. (Previously presented) A device according to claim 1, wherein the single crystal semiconductor substrate is a single silicon substrate.

29. (Currently amended) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein the impurity region is not in contact with the drain region, and

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region formed under the channel forming region and in the source region.

30. (Previously presented) A device according to claim 29, wherein the semiconductor device is an integrated circuit (IC).

31. (Previously presented) A device according to claim 29, wherein the semiconductor device is a microprocessor.

32. (Previously presented) A device according to claim 31, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

33. (Previously presented) A device according to claim 29, wherein the

semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

34. (Canceled) A device according to claim 29, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

35. (Withdrawn) A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity,

wherein a concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the impurity region is formed under the source region and the channel forming region while the impurity region is not formed under the drain region.

36. (Withdrawn) A device according to claim 35, wherein the semiconductor device is an integrated circuit (IC).

37. (Withdrawn) A device according to claim 35, wherein the semiconductor device is a microprocessor.

38. (Withdrawn) A device according to claim 37, wherein the microprocessor is at least one selected from the group consisting of a RISC processor an ASIC processor.

39. (With drawn) A device according to claim 35, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

40. (Withdrawn) A device according to claim 35, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.

41. (Withdrawn) A device according to claim 35,

wherein the second impurity is introduced from a direction of the <110> axis with respect t to the single semiconductor substrate.

42. (Currently amended) A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single crystal semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first

source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region and in the first source region;

wherein the first impurity region is not in contact with the first drain region,

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

43. (Previously presented) A device according to claim 42,

wherein the first n-type impurity is arsenic,

wherein the second n-type impurity is phosphorus,

wherein each of the first and second p-type impurity is boron.

44. (Previously presented) A device according to claim 42, wherein the semiconductor device is an integrated circuit (IC).

45. (Previously presented) A device according to claim 42, wherein the

semiconductor device is a microprocessor.

46. (Previously presented) A device according to claim 45, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

47. (Previously presented) A device according to claim 42, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

48. (Canceled) A device according to claim 42, wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

50. (Withdrawn) A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein a concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the impurity region is formed under the source region and the channel forming region while the impurity region is not formed under the drain region.

51. (Withdrawn) A device according to claim 50, wherein the semiconductor device is an integrated circuit (IC).

52. (Withdrawn) A device according to claim 50, wherein the semiconductor device is a microprocessor.

53. (Withdrawn) A device according to claim 52, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

54. (Withdrawn) A device according to claim 50, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

55. (Withdrawn) A device according to claim 50, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.

56. (Currently amended) An EL display device comprising:

a plurality of MOSFETs formed in a single crystal semiconductor substrate, each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region,

wherein the impurity region is not in contact with the drain region,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

57. (Currently amended) An EL display device according to claim 56,

wherein the first ~~n-type~~ impurity is arsenic, and

wherein the second ~~n-type~~ impurity is phosphorus~~, and~~.

~~wherein each of the first and second p-type impurities is boron.~~

58. (Previously presented) An EL display device according to claim 56, wherein the EL display device is incorporated into at least one selected from the group consisting of a cellular phone, a personal handy phone system and a portable computer.

59. (Canceled) An EL display device according to claim 56, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.